NASA TECHNICAL NOTE

NASA TN D-2317

AN EFFICIENT PCM ERROR CORRECTION AND SYNCHRONIZATION CODE

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JUNE 1964

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SUMMARY

An efficient method of frame synchronization and error correction is analyzed. The probability of frame synchronization as a function of single bit error probability is shown. Additional error correction information may be obtained if the voltage from the bit integrator is used with an error detecting code. The equivalent gain in signal-to-noise ratio, made by using the additional error correction method, is discussed. On the basis of this analysis, a ground station is proposed to process data by using these error correction techniques.

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INTRODUCTION

A communication system is proposed herein which uses biphase modulation to transmit binary information in serial form. When serial binary data transmission is used, identification is necessary so that the data can be regrouped into words or frames at the receiver. A synchronization code pattern is usually used for word or frame identification. With adequate synchronization assured the problem of errors occurring because of noise in the communication channel still remains. One method of reducing errors in the data output is to use an error correcting code.

This study was made to find an improved synchronization and error correction method for a one-way planetary landing probe communication system. A crossed parity check or iterated code (Reference 1) is used here since it lends itself to an intuitive understanding of the frame synchronization and error correction method. With a planetary landing probe, a limited quantity of data can be transmitted in a short time at a very high cost; therefore the data efficiency of the communication system should be as high as possible, and the amount of planetary probe communication electronics should be kept small to improve reliability. Finally, it is desirable to keep any necessary increase in system complexity in the ground station.

The frame synchronization and error correction codes are combined in this study for greater communication efficiency; however increased data processing is required at the receiver. A computer simulation is used to study the modified frame synchronization method and to make a set of curves for frame synchronization versus single-bit error probability. When an error detection code is used, additional error correction information is available at the receiver. The equivalent signal-to-noise ratio gain and the method of using this information is discussed.

FRAME SYNCHRONIZATION

Since measurements accurate to 1 percent of full scale are desired, the data are coded in 7 bit binary words. A horizontal parity bit is added to each 7 bit data word, making the total word length

*This report was presented at the National Space Electronics Symposium, Miami, Florida, October 1963, and published in the proceedings of that meeting.

8 bits. A number of 8 bit words are arranged in a matrix, as shown in Figure 1, with an 8 bit vertical parity word added on the bottom to complete the frame. The error correcting code is linear both vertically and horizontally, thus making an iterated code. In the computer simulation, frame sizes varying from 2 to 10 total words are studied.

Frame synchronization can be obtained by using the parity checks as if they were ones and zeros in a synchronization word (Reference 2). Parity checks may be assigned to be either even or odd, as desired, in the frame format. The data enters the receiver frame synchronizer in serial form. While the data shifts through the synchronizer, the data is checked for the formatted horizontal (X) and vertical (Y) parity. A frame synchronizer for a 3 word frame is shown in Figure 2. The number of X and Y parity disagreements or errors per serial bit shift are recorded. If the parity error count is searched to find low numbers of errors spaced one frame apart, then synchronization can be obtained reliably at single bit error probabilities less than 10^{-2}.

NOISE VOLTAGES READ FROM INTEGRATOR AT END OF BIT TIME WITH NO DATA BEING TRANSMITTED
(obtained from table of Gaussian deviates with $\mu = 0$ and $\sigma = 1/2.05$)

-0.225v	-0.094v	-0.006v	-0.590v	+1.049v	+0.652v	-0.960v	-0.862v
+0.711v	+0.431v	+0.488v	-0.082v	+0.408v	-0.603v	+0.796v	-0.693v
-0.936v	-0.608v	-0.102v	+0.381v	-0.161v	-1.441v	-0.218v	-0.046v

DATA WITH PROPER PARITY (to be transmitted) THE SYMBOL p SHOWS LOCATION OF PARITY BITS

0	1	0	1	0	0	1	1 p	EVEN
1	1	0	0	1	1	0	1 p	ODD
0 p	1 p	0 p	0 p	0 p	1 p	1 p	0 p	ODD
ODD	ODD	EVEN	ODD	ODD	EVEN	EVEN	EVEN	

SIGNAL PLUS NOISE VOLTAGE AS RECEIVED WITH THE CORRESPONDING PROBABILITY OF EACH BIT BEING IN ERROR

-1.225v $3.6X10^{-5}$	+0.906v $4.7X10^{-4}$	-1.006v $2.2X10^{-4}$	+0.410v $3.0X10^{-2}$	+0.049v $3.9X10^{-1}$	-0.348v $4.8X10^{-2}$	+0.040v $4.1X10^{-1}$	+0.138v $2.3X10^{-1}$	C
+1.711v $5.6X10^{-7}$	+1.431v $5.8X10^{-6}$	-0.512v $1.3X10^{-2}$	-1.082v $1.1X10^{-4}$	+1.408v $7.2X10^{-6}$	+0.397v $3.3X10^{-2}$	-0.204v $1.4X10^{-1}$	+0.307v $6.6X10^{-2}$	
-1.936v $8.6X10^{-8}$	+0.392v $3.8X10^{-2}$	-1.102v $9.2X10^{-5}$	-0.619v $5.2X10^{-3}$	-1.161v $5.6X10^{-5}$	-0.441v $2.3X10^{-2}$	+0.782v $1.3X10^{-3}$	-1.046v $1.5X10^{-4}$	D
				A	B			

Figure 1—Three word frame with a signal-to-noise ratio of 6.2 db in a bandwidth of one-half the bit rate.

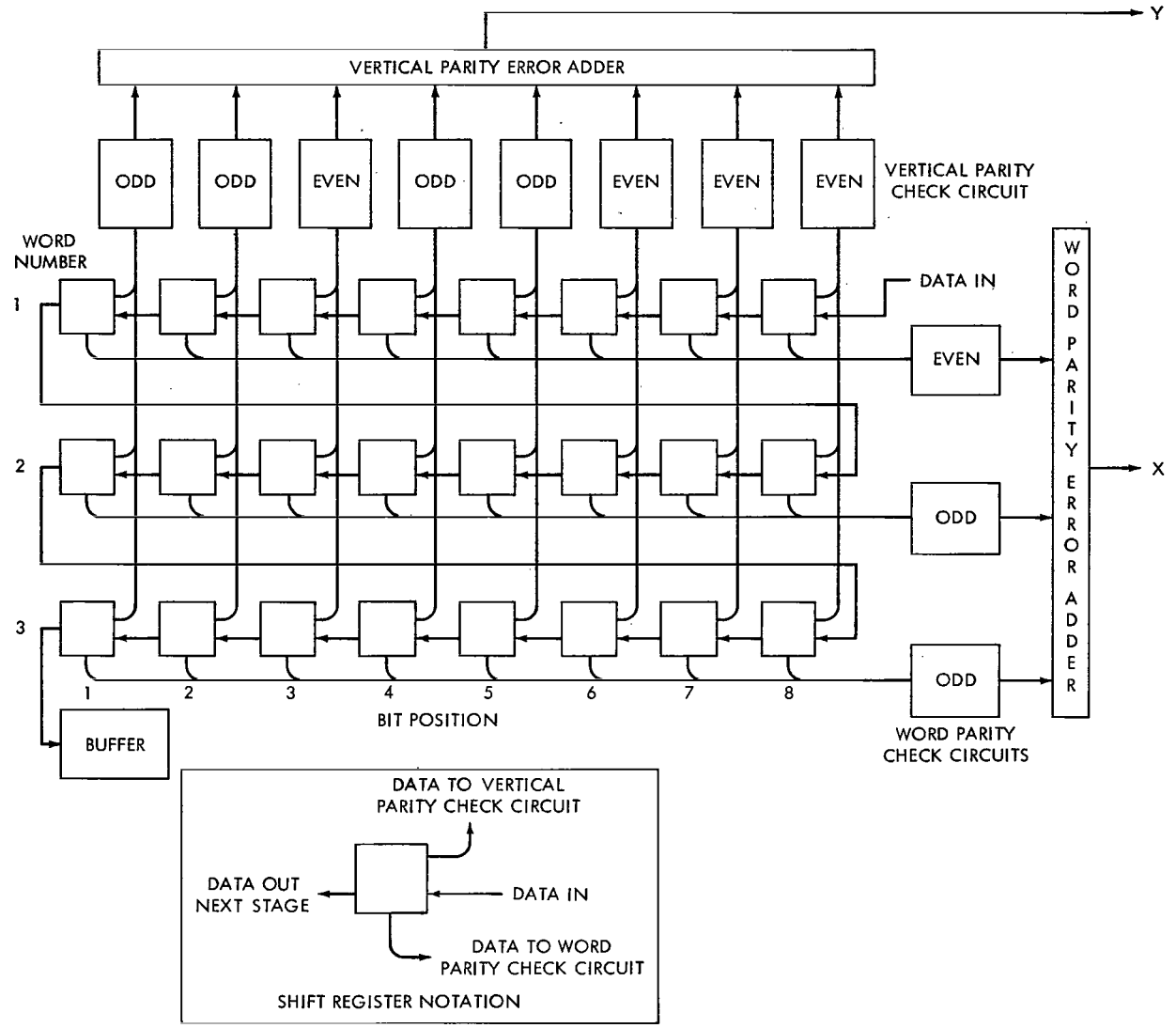

Figure 2—Frame synchronization system.

To determine the synchronization capabilities of this code a computer simulation was performed. A constant bit rate and a random error probability were assumed. The effect of bit synchronization extending into noise on either or both ends of the data was considered.

The computer program generates up to forty frames of serial bits as if they were the output of a bit synchronizer. The bits are produced by a random number generator. Frames of data differ from frames of noise only in that bits are arranged in the right-hand column and bottom row to satisfy the parity requirements. Both X and Y parity structures must be specified for each test as if they were synchronization words. Data frames followed and preceded by noise frames are produced with the number in each group being a specified integer. Random errors are then added, as if the errors had occurred because of additive white noise in the transmission path, by randomly complementing bits at a specified error rate.

Any combination of four output routines may be called for in the computer simulation. In routine one the sequence of frames is printed out before and after the errors are added; in addition a listing of the error positions is printed out. Routine two analyzes the number of X and Y parity errors and prints a line each time the number of errors in X or Y or their sum is less than a specified threshold. This threshold is used to limit the amount of data output from the computer. Each line of printout gives the bit position measured from the first bit in the series, the number and location of the X and Y parity errors, and the number of bit positions between this match and the preceding fifteen lines of printout. This routine was used to establish the synchronization rule to be used in the next section. Each potential series of frames in routine three is given an identity number and a point count on the output. The series with the highest point count is assumed to be the correct synchronization series. Figure 3 also shows a "no synchronization" curve which corresponds to two or more series having the same point count. The fourth routine complements each bit before it enters the bit synchronizer and has the same output as routine three. Inversion of the data can only be discovered by using an odd number of words in a frame and checking the normal and inverted Y parity sequences.

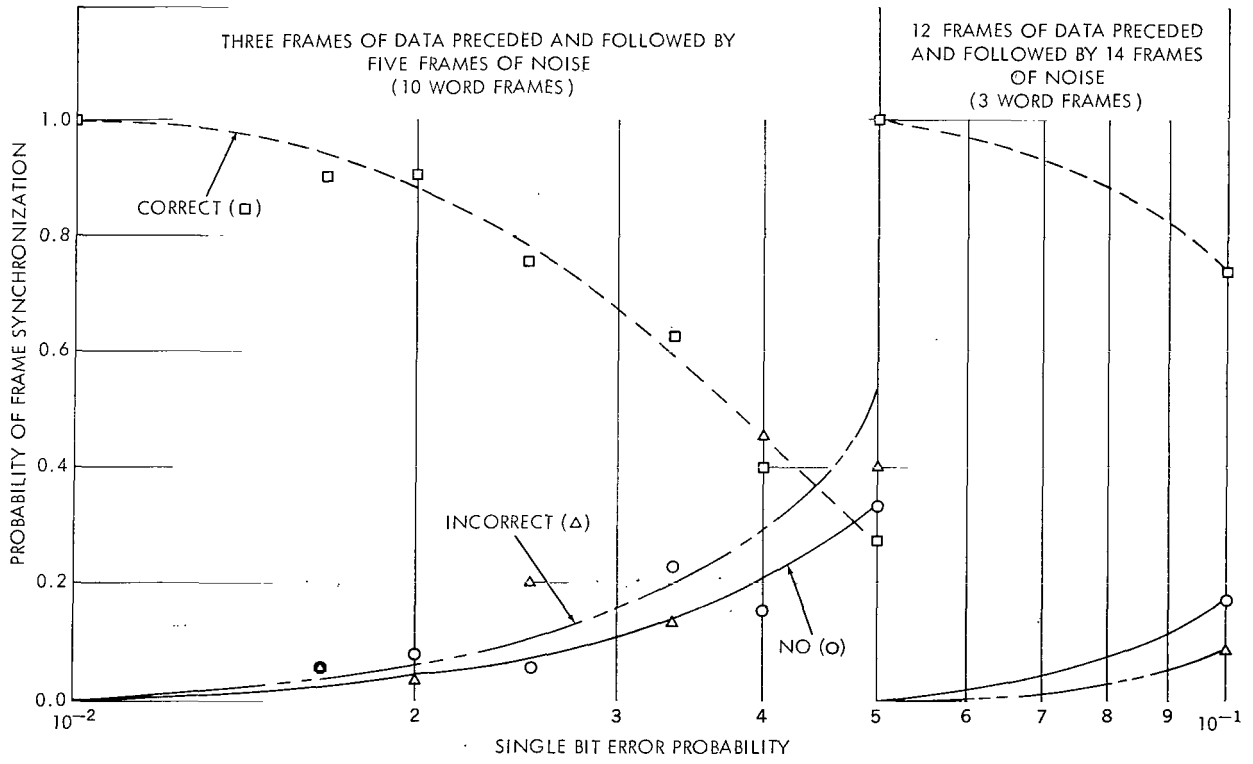

Figure 3—Frame synchronization probability.

COMPUTER SYNCHRONIZATION RULE

The synchronization rule used in routines three and four requires that the starting frame have less than three X and Y errors without having been used in any previous series. If the

starting frame is the only one in a series, then it will be deleted from the output. Once a starting frame has been found, the two preceding frames, spaced one and two frame lengths away, as well as all succeeding frames in this synchronization pattern, multiples of one frame length away, are checked for the number of parity errors. When two succeeding frames having more than two X or Y errors are found, the series is ended. All frames in a series having less than three X and three Y errors are given one of the following point counts:

1. Number of X and Y errors unequal, -1
2. Three X and three Y errors, 1
3. Two X and two Y errors, 2
4. One X and one Y error, 3
5. Zero X and zero Y errors, 4

If a frame having more than three X or Y errors is encountered between two frames in a series, the point count is reduced by 1. The point count is summed for all the frames in a series to give the total point count which appears on the output.

With an error probability of 2×10^{-2}, the computer simulation showed a 90 percent probability of correct synchronization on a group of three 10 word frames preceded and followed by five frames of noise (see Figure 3). When the same amount of data is sent using 3 word frames, the probability of finding the synchronization series at an error rate of 10^{-1} is 75 percent; however, it is more difficult to determine where the data starts and stops with relation to the noise.

Using an odd number of words in a frame proved to be a reliable method of telling whether the data bits had been complemented during transmission.

Since data with a single bit error probability of less than 10^{-3} are expected and frame synchronization is acquired reliably at an error probability of 10^{-2}, it is felt that an adequate frame synchronization margin has been provided. In the section on error correction, perfect frame synchronization is assumed. This assumption is invalid at error probabilities greater than 10^{-2}. A single bit error probability of 10^{-2} is therefore used as an upper bound in the error correction study.

ERROR CORRECTION

Error Correction Advantages

The crossed parity structure used in this study for frame synchronization and error correction has a minimum Hamming distance of 4. With a Hamming distance of 4 an even number of errors having a distance of 4 or greater can go undetected in a frame. Fortunately, a frame having the number of errors necessary to produce an undetectable error condition seldom has the errors lying in an undetectable pattern. Within the error probability range of interest —single bit error probabilities less than 10^{-2} — the binomial probability of increasing numbers of errors

in a frame approaches zero with sufficient rapidity to cause the probability of 4 or more errors in a 10 word frame to be less than 10^{-2}. If all the frames with 4 or more errors were falsely corrected, less than 1 percent of the frames would be affected.

Since the iterated code is being used for single error correction, there is the danger of changing some of the odd numbers of errors into an undetectable even number of errors. When error correction is used, the gain in correct data must not be offset by a comparable gain in bad data. Since the tables of binomial probability distribution show that no difficulty will result from using single error correction or even dual and triple error correction, it is safe to use the code under discussion. Figures 4 and 5 show the probability of a frame being in error after single and dual error correction, respectively. The single frame error probability is plotted against signal-to-noise-power ratio in a bandwidth equal to the information bit rate for three different frame sizes. The relationship between bit rate and information bit rate is determined as follows:

The bit rate BR = N/T and the information bit rate IBR = K/T, where N is the total number of bits in a frame, T is the total frame transmission time, and K is the number of information bits

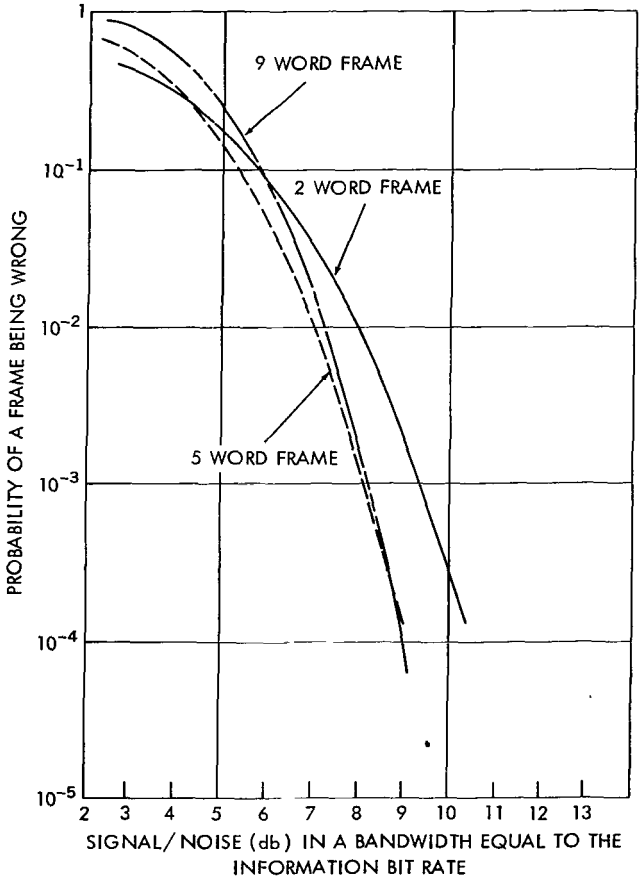

Figure 4—Single frame error probabilities, single error correction. The information rate is held constant.

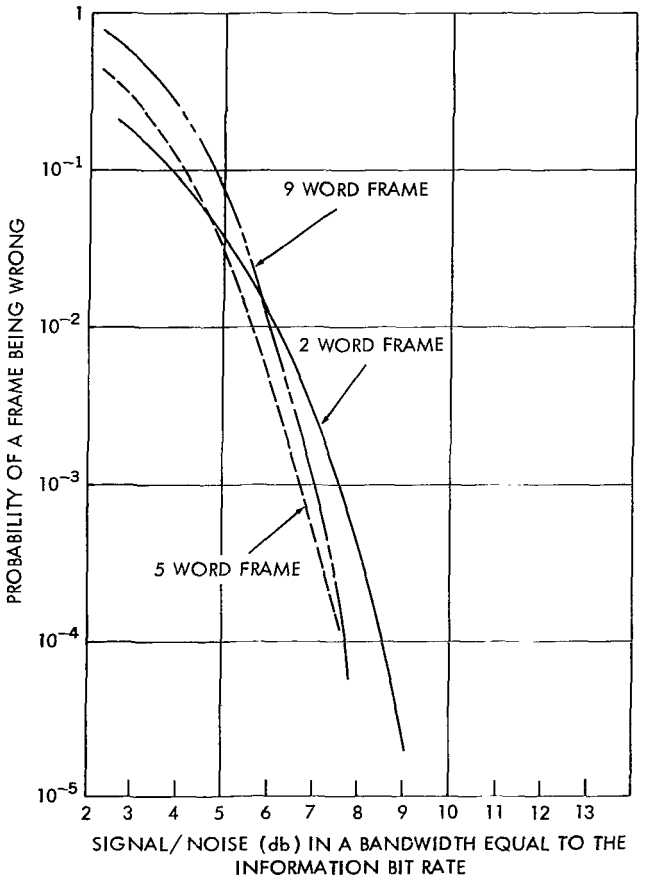

Figure 5—Single frame error probabilities, dual error correction. The information rate is held constant.

in a frame. Thus

$$\frac{IBR}{BR} = \frac{K}{N} .$$

When frame sizes are compared, a constant information bit rate is used to find the highest probability of correctly receiving data. This is done in order to receive the maximum amount of information per unit time without regard to the code efficiency K/N. The efficiency and consequently the bit rate is varied by changing the frame size. A point on Figure 4 may be determined in the following manner. Since odd values are not found in the binomial probability distribution tables (Reference 3) start with a convenient single bit error probability. If a single bit error probability of 10^{-2} is chosen as the starting value, then a cumulative binomial probability of 0.16229 is found for two or more errors in a 9 word frame which corresponds to single bit error correction. The binomial probability value is plotted on the ordinate of Figure 4, but the abscissa value still remains to be found. For a matched filter bit detector a single bit error probability of 10^{-2} corresponds to a 7.35 db signal-to-noise ratio in a bandwidth equal to half the bit rate or a 4.34 db signal-to-noise ratio in a bandwidth equal to the bit rate. Going from the bit rate bandwidth to the information bit rate bandwidth produces a gain in signal-to-noise ratio equal to N/K. For the 9 word frame the N/K ratio is 1.286 which corresponds to a gain of 1.09 db. The single frame error probability of 0.16229 for the 9 word frame corresponds to a 5.43 db signal-to-noise ratio in a bandwidth equal to the information bit rate. In Figure 4 all the frames have been adjusted to have the same information bit rates with the same noise density in the communication channel. This means that the 2 word frame must have a bit rate 1.78 times that of the 9 word frame and, consequently, a higher single bit error probability. Even though the 2 word frame has the highest single bit error probability associated with it, fewer bits are in the 2 word frame, decreasing the probability of an error occurring in the frame. The 2 word frame also has the highest ratio of bit correction capability to data bits in the frame. These two effects work together to make the single frame probability of an error for the 2 word frame less than the error probabilities of the larger frames at low signal-to-noise ratios. The superior error correction capability of the 2 word frame is not as valuable at high signal-to-noise ratios and, therefore, the single frame error probability curve of the 2 word frame drops below the larger-frame error probability curves. It must be kept in mind that Figures 4 and 5 show single frame error probabilities, and it takes eight 2 word frames or two 5 word frames to equal the same amount of data contained in one 9 word frame.

Determination of Conditioned Bit Error Probability

More correction capability is available in a system using a matched filter bit detector with an error detecting code than can be achieved by using a simple one-zero decision corresponding to a plus or minus voltage polarity from the bit detector. The added information available from the bit detector may be obtained by recording not only the polarity but also the magnitude of the voltage from the integrator at the end of the bit time. The probability of a bit being in error would be expected to decrease as the bit voltage increases. This is true because it is unlikely that a large

integrator voltage is due to a bit voltage polarity having been changed, which causes an error, and further increased due to noise alone. The probability of interest, $P(e/|v|)$, is the conditional probability of an error having occurred if the absolute value of the integrator voltage is given. The absolute value of the integrator voltage is used because both polarities of voltage will produce the same result in the derivation. The Gaussian probability densities, due to white noise, of ones $p^1(v)$ and zeros $p^0(v)$ are symmetrically placed about zero volts and have the same standard deviation (Figure 6). Ones and zeros are assumed to have equal probabilities of occurrence in the following discussion. $P(e/|v|)$ is

$$P(e/|v|) = \frac{P(e|v|)}{P(|v|)} , \tag{1}$$

where $P(e|v|)$ is the joint probability of having an error and having the voltage $|v|$ present due to the probability density $p^E(v)$ (Figure 7),

$$P(e|v|) = p^E(v)\,\Delta v . \tag{2}$$

$P(|v|)$ is the probability of finding the voltage $|v|$ due to probability densities $p^E(v)$ and $p^C(v)$ combined,

$$P(|v|) = p^E(v)\,\Delta v + p^C(v)\,\Delta v . \tag{3}$$

If $|\mu|$, which is both the mean of the noise distribution and the amplitude of the signal level, is found, then all the voltage readings obtained can be normalized and no loss of generality results from using a normalized mean of ± 1 in the Gaussian probability density distributions. The distribution $p^E(v)$ is the tail of the density function and indicates an error condition; $p^C(v)$ is the main body of the density function associated with a correct bit,

$$p^E(v) = \frac{1}{\sqrt{2\pi}\sigma} e^{-(v+1)^2/2\sigma^2} , \tag{4}$$

$$p^C(v) = \frac{1}{\sqrt{2\pi}\sigma} e^{-(v-1)^2/2\sigma^2} . \tag{5}$$

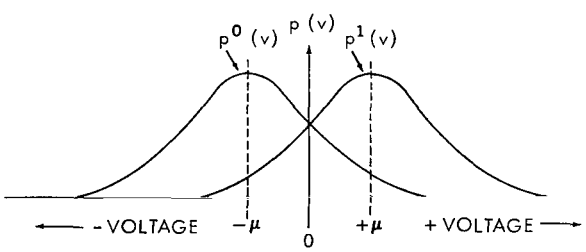

Figure 6—Noise pulse signal probability densities.

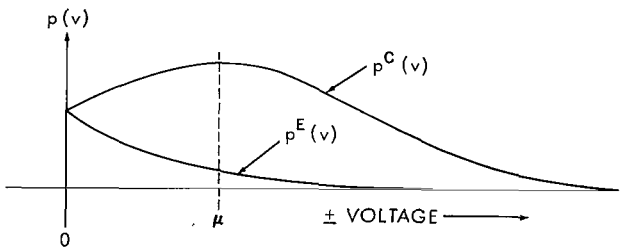

Figure 7—Correct bit and error bit probability densities.

Substituting Equations 2 and 3 into Equation 1 shows

$$P(e/|v|) = \frac{p^E(v)\,\Delta v}{p^E(v)\,\Delta v + p^C(v)\,\Delta v} . \tag{6}$$

Then by substituting Equations 4 and 5 into Equation 6 and simplifying,

$$P(e/|v|) = \frac{e^{-v/\sigma^2}}{e^{-v/\sigma^2} + e^{v/\sigma^2}} = \frac{e^{-v/\sigma^2}}{2\cosh\frac{v}{\sigma^2}} . \tag{7}$$

If $v/\sigma^2 > 4$ this simplifies to:

$$P(e/|v|) \approx e^{-2v/\sigma^2} . \tag{8}$$

A plot of $P(e/|v|)$ is shown as a function of bit detector voltages for several different values of signal-to-noise ratio in Figure 8.

Computation of μ and σ

A significant sample of bit voltages must be chosen but not so large a sample that a changing μ and σ will be averaged. The mean μ of the Gaussian density function must be found first. In a binary system the density functions for ones and zeros add together in the receiver and cannot be separated. The Gaussian mean cannot be found directly, but a good approximation results if the absolute value of the integrator voltage is used to compute a mean:

$$\mu' = \frac{2\sigma}{\sqrt{2\pi}} e^{-\mu^2/2\sigma^2} + 2\mu\left(\frac{1}{\sqrt{2\pi}}\int_0^{\mu/\sigma} e^{-y^2/2}\,dy\right) . \tag{9}$$

If μ'/μ is calculated through the range of interest of σ, it is found that $\mu \approx \mu'$. The standard deviation can be calculated by standard methods since it is not affected by the change in the density function if the Gaussian mean is known. With the mean equal to 1, the standard deviation σ is equal to the reciprocal of the signal-to-noise rms voltage ratio (for a bandwidth equal to half the bit rate for a matched filter bit detector).

The Multiple Error Correction Procedure

Multiple bit error correction can be achieved with the iterated code under discussion in conjunction with the conditional bit error probability $P(e/|v|)$. The position and number of parity errors must be inspected to determine all the possible configurations of errors for each possible number of errors in a frame. For example, two errors may occur in three basic ways: both may be in the same row (two Y errors, no X errors), the same column (two X errors, no Y errors), or different rows and columns (two X and two Y errors). If any of the above parity error conditions

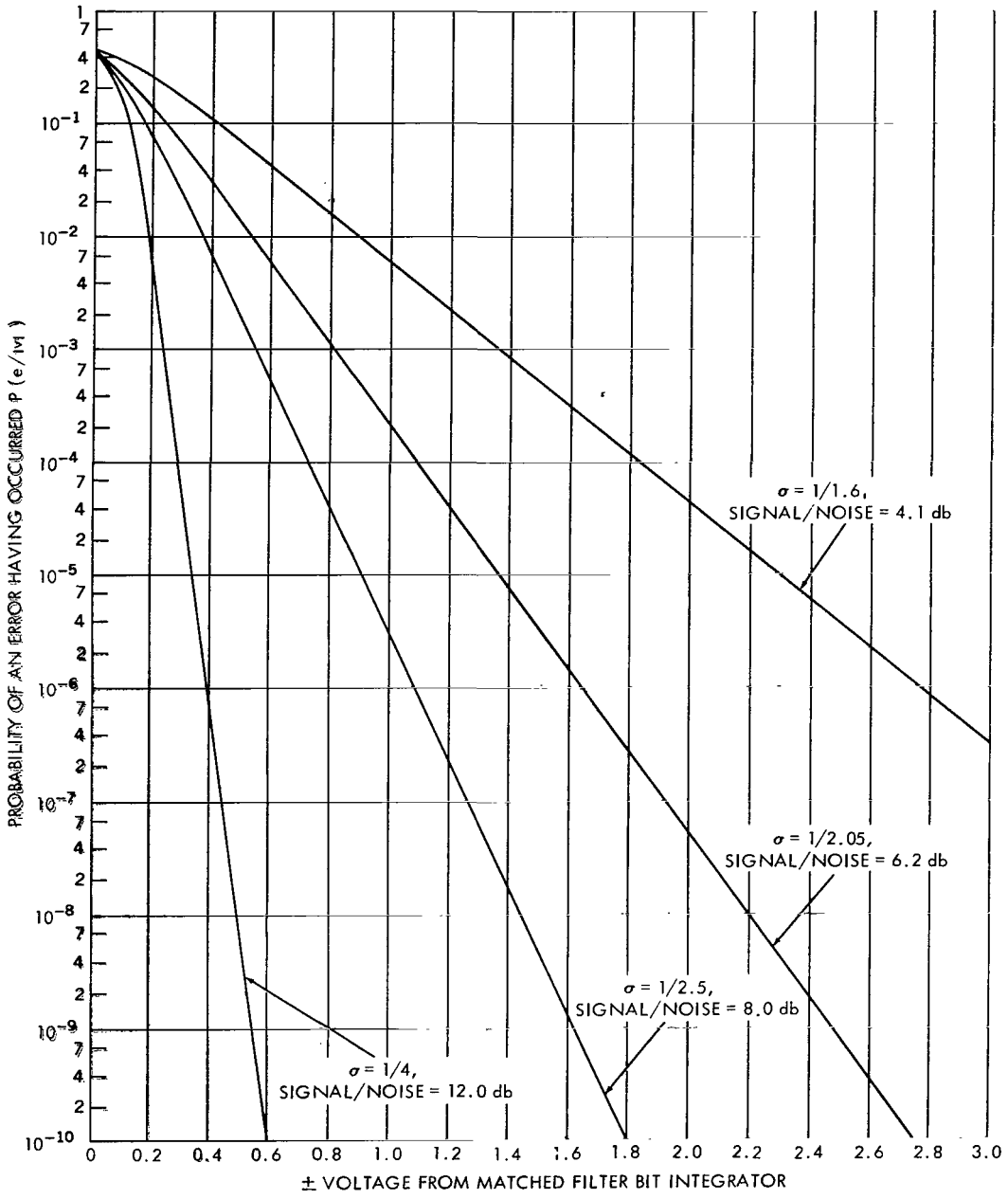

Figure 8—Voltage-conditioned error probability. $P(e/|v|) = e^{-v/\sigma^2/2} \cosh v/\sigma^2$. The voltage from the integrator has been divided by μ. The value of the signal-to-noise ratio is for a bandwidth of one-half the bit rate.

are found, two errors are assumed to exist in the frame. This assumption is not necessarily valid but, as previously explained, will not result in a significant amount of the data being degraded.

A specific example showing how two errors could occur in a 3 word frame is shown in Figure 1. The parity used for the data of Figure 1 is the same as that shown in the frame synchronizer

of Figure 2. The noise voltages without data, shown in Figure 1, are obtained by using a table of Gaussian deviates having a mean of zero and a standard deviation of one. The standard deviation is then adjusted to the case of interest by multiplying each value obtained from the Gaussian deviate table by the desired standard deviation. In Figure 1 the standard deviation σ was set equal to 1/2.05, which is the reciprocal of the signal-to-noise rms voltage ratio in the bandwidth shown. This signal-to-noise ratio leads to a single bit error probability of 2×10^{-2}. A high error probability is used so that it is not necessary to wait long for two errors to occur.

If the data of Figure 1 were transmitted without noise, the voltage appearing on the integrator at the end of a bit time would be +1 volt for a one and -1 volt for a zero. The receiver bit detector is assumed to be linear so that superposition may be used to find the result of signal plus noise. The bottom chart of Figure 1 shows the data bit voltages as received. The voltage polarity indicates whether a one or zero has been received, + for a one and – for a zero. By comparing the bits to be transmitted with those received, it is found that errors have occurred at AC and BD.

In using the proposed error correction method, first the probability of each bit being in error is found from Figure 8 and then placed with its corresponding voltage. The parity errors indicate a dual error is most likely and lies either in AC and BD or in AD and BC. The conditional probability of each error is found:

$$P(e/0.049V) = 3.9 \times 10^{-1}, \text{ position AC} \tag{10}$$

$$P(e/0.348V) = 4.8 \times 10^{-2}, \text{ position BC} \tag{11}$$

$$P(e/1.161V) = 5.6 \times 10^{-5}, \text{ position AD} \tag{12}$$

$$P(e/0.441V) = 2.3 \times 10^{-2}, \text{ position BD} \tag{13}$$

The joint probability of errors AC and BD is found by using Equations 10 and 13

$$P(\text{AC and BD}) = 8.97 \times 10^{-3} \tag{14}$$

The joint probability of errors BC and AD is found by using Equations 11 and 12

$$P(\text{BC and AD}) = 2.69 \times 10^{-6} . \tag{15}$$

The results of Equations 14 and 15 show that the dual error is most probably in AC and BD. This method of error correction has an error probability as a function of the signal-to-noise ratio associated with it. The probability of incorrectly "correcting" a frame may be calculated in a manner similar to that used for a multiple channel or character error probability calculation (Reference 4). Figure 9 shows that the equivalent gain in signal-to-noise ratio for equal error

probabilities between single and dual error correction for the 2 word frame is approximately 1.8 db. If all errors detected by the crossed parity check are corrected, the maximum possible gain in equivalent signal-to-noise ratio is about 6 db.

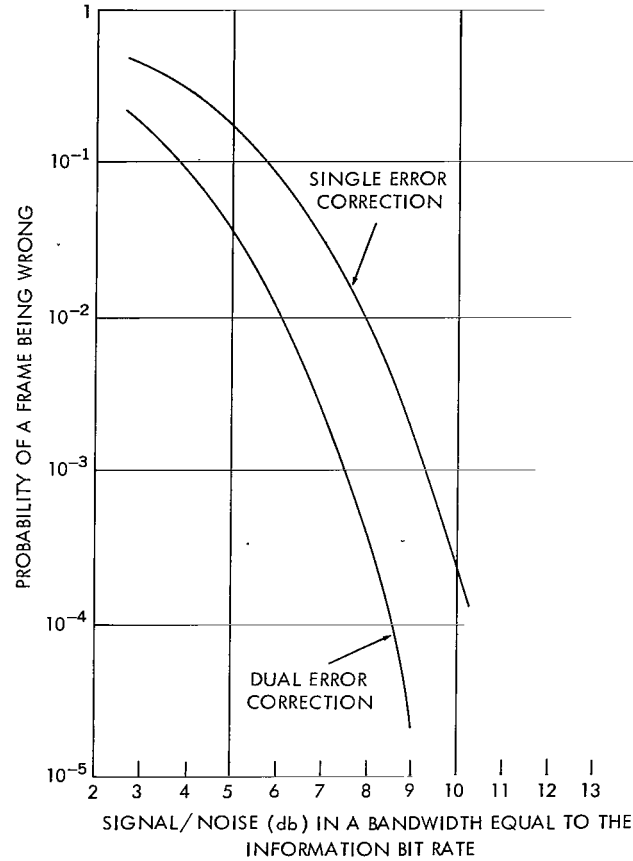

Figure 9—Two word frame error probability.

GROUND STATION CHARACTERISTICS

The proposed organization of a ground station to process this type of data is shown in Figure 10. The output of the receiver is a noisy biphase modulated coherent subcarrier. Conventional techniques of doubling, filtering, halving, and again filtering are used to reconstruct a subcarrier which is either in phase or 180 degrees out of phase with the received signal. The output of the multiplier is then noise plus a square wave PCM signal. Data is encoded with the Manchester Code in which the phase of the subcarrier is reversed in the center of each bit time. This leads to a high transition density in the bit stream so that the bit timing detector can rapidly establish a bit timing rate equal to twice the information bit rate. The voltage on the matched filter integrator is measured by the analog-to-digital converter just prior to the capacitor being discharged, and the value is transferred into a small computer. As soon as a few transitions between ones and zeros are detected in the data, the computer can establish the proper phasing of the information bit rate data within the double bit rate data. To establish the voltage that would have been on the integrator if more conventional coding had been used, the voltage on the integrator at the center of the bit time is added to the complement of the voltage on the integrator at the end of the bit time. No penalty is incurred by running the bit synchronizer at twice the information bit rate, since the signal is integrated in the proper phase over the full information bit time. If this voltage is positive, an "A" has been detected, and if negative, a "Not A" has been detected. It is not possible at this stage in the processing to state if A is a one or zero since the method of generating the local subcarrier destroys this information.

The computer is used to establish frame synchronization and to determine whether an A is a one or zero. There will only be a parity correlation for one of these cases since a frame with an odd number of words will be used and complementing all of the bits destroys the specified parity structure. The printed output of this computer will be frame-synchronized data indicating the rows and columns in which parity errors occur. The output voltage of the integrator for each bit

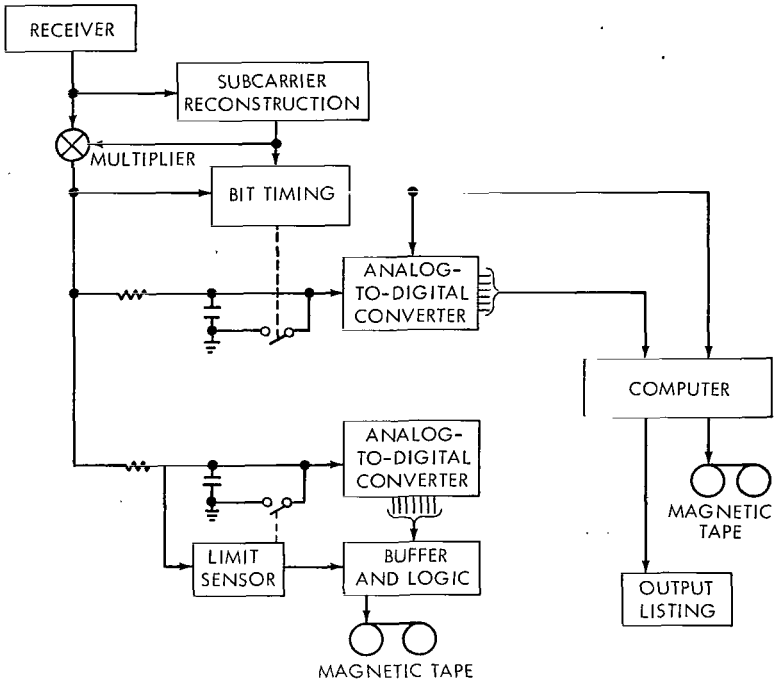

Figure 10—Proposed ground station.

is presented so that the previously described error correction procedures may be used if more than one error occurs. This output will be made available in real time and will lag the incoming data by about three frame transmission times. A small computer with a memory of 4096 words of 12 bits each, operating at a rate of about 10,000 additions per second could easily perform the computations necessary to synchronize the data. The operational rate would be about 2 bits per second with a bench test rate of 10 bits per second in a good signal-to-noise ratio environment.

Data will be lost in the system described above during the time that the bit timing detector is establishing the proper timing. In order not to lose this data and to be able to operate in a noise environment where it may be excessively difficult to establish bit timing rapidly, another system will be used to acquire data for nonreal time processing. The output of the multiplier will go to an integrator which continuously integrates this voltage. A limit sensor detects whether this integrator is approaching its voltage limit ranges and resets the voltage to zero. The voltage on the integrator will be digitized at about 20 samples per bit time along with information about the voltage reset pulses that may have been used. In an off-line process the contents of the integrator can be reconstructed if the voltage reset times are known. Bit timing may be established by cross correlation techniques. After the subcarrier reconstruction unit establishes phase lock between the noisy incoming signal and its output, all of the data can be recovered in an optimum manner. The ratio between the subcarrier frequency and bit rate will be over 250 to 1; therefore very few bits will be lost during the time that the subcarrier reconstruction unit is acquiring phase lock.

CONCLUSIONS

The crossed parity structure is effective in establishing frame synchronization of the data and in providing an error detecting and correcting code. Frame synchronization can be established at error rates such that the majority of the data could not be corrected. The extension of the error correction process, by measuring the voltage on the integrator at the sample time (from single bit to multiple bit error correction) is effective and is a powerful tool with application to many other codes. This technique allows a significant increase in the probability of getting correct data after the error correction process is completed without increasing the complexity of the data encoder. The ground station used to recover data in this form is best implemented with the aid of a small computer.

ACKNOWLEDGMENTS

The authors are indebted to Joseph D. Barksdale who programmed the IBM 7090 to test the frame synchronization method and to obtain data for Figure 3.

(Manuscript received October 29, 1963)

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